

Title: Lab Course RISC-V Processor Design

Course description

Prerequisite: Computer Architecture and Organisation (CAO)

Details: In this lab course, the students will learn to design and implement a RISC-V processor on a Field Programmable Gate Array (FPGA). The modern state of the art hardware structures found in the processors will be adapted in the design of combinatorial and sequential circuits. The students will learn the importance of the concepts of pipelining, Finite State Machine (FSM) and interrupts in optimising the synthesis. At the end, a project would be assigned which would involve the concepts covered throughout the course.

Goal: The students will be able to design digital circuits on hardware (FPGA) using design automation tool (Vivado). They will also learn to work in a team.

Teaching language: English